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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/785,500	02/20/2001	Kumiko Takikawa	ASA-964	6528

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EXAMINER

YUN, EUGENE

ART UNIT PAPER NUMBER

2682

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

11/11

Office Action Summary	Application No. 09/785,500	Applicant(s) TAKIKAWA ET AL.	
	Examiner Eugene Yun	Art Unit 2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 February 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>3/21/05</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson et al. (US 6,510,309) in view of Tanaka (JP 57-43453) and Matsubara (JP 02-142185 "IDS").

Referring to Claim 1, Thompson teaches a wireless communications system comprising:

A filter 38 (fig. 2);

A semiconductor chip including a signal processing integrated circuit (see col. 4, lines 20-22) having an amplifier 62 (fig. 2) for receiving an output signal from said filter 42 (fig. 2);

Wherein a main surface of said semiconductor chip is provided with a plurality of electrode terminals along an edge portion thereof (see fig. 3 where it is known in the art that all semiconductor chips include a plurality of electrode terminals along an edge portion thereof); and

Wherein said amplifier has a transistor 200 (fig. 5) including a control electrode to which the output signal of said filter is to be supplied, a first electrode through which a signal is outputted in accordance with the signal supplied to said control electrode, and

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a second electrode to which a voltage is applied (see 200 of fig. 5 noting that the electrodes simply describe the emitter, collector, and base of a transistor).

Thompson does not teach the control electrode, first electrode, and second electrode of said transistor connected to said electrode terminals through wirings, respectively.

Tanaka teaches the control electrode, first electrode, and second electrode of said transistor connected to said electrode terminals through wirings, respectively (see fig. 4 where the transistor is connected directly to the pads 2, 6, and 7 also shown along the edges in fig. 5 noted by reference numbers 2', 6' and 7'). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Tanaka to said system of Thompson in order to maintain voltage gain in the circuit.

The combination of Tanaka and Thompson does not teach that none of said wirings are arranged to traverse said wirings respectively connected between a first said electrode terminal and said first electrode of said transistor, between a second said electrode terminal and said second electrode of said transistor, and between a third said electrode terminal and said control electrode of said transistor. Matsubara teaches that none of said wirings are arranged to traverse said wirings respectively connected between a first said electrode terminal and said first electrode of said transistor, between a second said electrode terminal and said second electrode of said transistor, and between a third said electrode terminal and said control electrode of said transistor (see figs. 1, 5, and 6 where it is clear that none of said wirings traverse). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide

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the teachings of Matsubara to said system of Thompson in order to reduce parasitic inductance in a wireless IC.

Referring to Claim 2, Tanaka also teaches said semiconductor chip having said edge portion and an opposite side to said edge portion, and said electrode terminals, said transistor and a wiring through which a voltage is supplied to said transistor are in turn arranged from said edge portion towards said opposite side (see fig. 4).

Referring to Claim 3, Thompson also teaches the voltage supplied to said second electrode terminal of said transistor as a ground voltage, and the second electrode terminal through which the ground voltage is supplied to said second electrode terminal of said transistor is different from one of the electrode terminal through which the ground voltage is supplied to electrostatic discharge protecting circuits provided for said transistor (see 200 of fig. 5 where one electrode is connected to ground).

Referring to Claim 4, Tanaka also teaches a signal transmitting circuit and the wiring through which a voltage is supplied to said signal transmitting circuit is coupled to the same one of the electrode terminals as that of the wiring through which a voltage is supplied to a bias circuit and said electrostatic discharge protecting circuits for said amplifier (see pad 7 in fig. 4).

Referring to Claim 5, Tanaka also teaches said amplifier present on said edge portion of said semiconductor chip and arranged near the center of said edge portion (see fig. 5).

Referring to Claim 6, Tanaka also teaches said amplifier arranged at a corner part which is defined between said edge portion of said semiconductor chip and a crossing side which crosses said one edge portion (see pads 2', 6', and 7' in fig. 5).

Referring to Claim 7, Tanaka also teaches no wiring arranged between said electrode terminals and said edge portion of said semiconductor chip (see fig. 4).

Referring to Claim 8, Tanaka also teaches the wiring arranged from said electrode terminal linked with said control electrode of said transistor and one electrode of protection diodes which are provided for said transistor (see fig. 4 where it is known in the art that protection diodes are provided in most transistors today).

Referring to Claim 9, Tanaka also teaches said amplifier arranged between said edge portion of said semiconductor chip and said electrostatic discharge protecting circuit (see figs. 4 and 5).

Referring to Claim 22, Matsubara also teaches said semiconductor chip including electrostatic discharge protecting circuits connected through a first wiring to said plurality of electrode terminals connected with said transistor, and wherein none of said wirings, except for said first wiring, are arranged to traverse said wiring connected between said first electrode terminal and said first electrode of said transistor, between said second electrode terminal and said second electrode of said transistor, and between said third electrode terminal and said control electrode of said transistor (see figs. 1, 5, and 6 where it is clear that none of said wirings traverse).

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3. Claims 10-13, 15-21, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson, Matsubara and Tanaka in view of Lysejko et al. (US 6,298,246).

Referring to Claim 10, Thompson teaches a wireless communications system comprising:

A filter 38 (fig. 2);

A semiconductor chip including a signal processing integrated circuit (see col. 4, lines 20-22) having an amplifier 62 (fig. 2) for receiving an output signal from said filter 42 (fig. 2);

Wherein a main surface of said semiconductor chip is provided with a plurality of electrode terminals along an edge portion thereof (see fig. 3 where it is known in the art that all semiconductor chips include a plurality of electrode terminals along an edge portion thereof); and

Wherein said amplifier has a transistor 200 (fig. 5) including a control electrode to which the output signal of said filter is to be supplied, a first electrode through which a signal is outputted in accordance with the signal supplied to said control electrode, and a second electrode to which a voltage is applied (see 200 of fig. 5 noting that the electrodes simply describe the emitter, collector, and base of a transistor).

Thompson does not teach the control electrode, first electrode, and second electrode of said transistor connected to said electrode terminals through wirings, respectively.

Tanaka teaches the control electrode, first electrode, and second electrode of said transistor connected to said electrode terminals through wirings, respectively (see fig. 4

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where the transistor is connected directly to the pads 2, 6, and 7 also shown along the edges in fig. 5 noted by reference numbers 2', 6' and 7'). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Tanaka to said system of Thompson in order to maintain voltage gain in the circuit.

The combination of Tanaka and Thompson does not teach that none of said wirings in each of said signal processing integrated circuits are arranged to traverse said wirings respectively connected between first ones of said electrode terminals and said first electrodes of said transistors, between second ones of said electrode terminals and said second electrodes of said transistors, and between third ones of said electrode terminals and said control electrodes of said transistors. Matsubara teaches that none of said wirings in each of said signal processing integrated circuits are arranged to traverse said wirings respectively connected between first ones of said electrode terminals and said first electrodes of said transistors, between second ones of said electrode terminals and said second electrodes of said transistors, and between third ones of said electrode terminals and said control electrodes of said transistors (see figs. 1, 5, and 6 where it is clear that none of said wirings traverse). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Matsubara to said system of Thompson in order to reduce parasitic inductance in a wireless IC.

The combination of Thompson, Matsubara, and Tanaka does not teach the wireless communication system comprising two signal processing circuits having different

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wavelengths. Lysejko teaches the wireless communication system comprising two signal processing circuits having different wavelengths (see col. 5, lines 34-43).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Lysejko to said system of Thompson in order to better withstand pressure to varying climatic conditions.

Referring to Claim 11, Tanaka also teaches said semiconductor chip having said edge portion and an opposite side to said edge portion, and said electrode terminals, said transistor and a wiring through which a voltage is supplied to said transistor are in turn arranged from said edge portion towards said opposite side (see fig. 4).

Referring to Claim 12, Thompson also teaches the voltage supplied to said second electrode terminals of said transistor as a ground voltage, and the second electrode terminals through which the ground voltage is supplied to said second electrode terminals of said transistors is different from the electrode terminals through which the ground voltage is supplied to electrostatic discharge protecting circuits provided for said transistors (see 200 of fig. 5 where one electrode is connected to ground).

Referring to Claim 13, Thompson also teaches each amplifier of said signal processing systems and said electrostatic discharge protecting circuits connected to said amplifier are provided in one area (fig. 2);

Said one area has a contour which is surrounded with a side extending along said edge portion of said semiconductor chip, and opposite side opposite to said edge portion and sides linking said edge portion with said opposite side (fig. 3); and

Said opposite side is of a power source line and a ground line of a contour which is changed step by step (fig. 5).

Referring to Claim 15, Thompson also teaches said amplifier of each of said signal processing systems and said electrostatic discharge protecting circuits connected to said amplifier are provided in one area (fig. 2);

Said one area is provided at a predetermined interval between said edge portion of said semiconductor chip, and opposite side opposite to said edge portion (fig. 3); and

Said opposite side is of a power source line and a ground line of a contour which is changed step by step (fig. 5).

Referring to Claim 16, Tanaka also teaches a signal transmitting circuit and the wiring through which a voltage is supplied to said signal transmitting circuit is coupled to the same electrode terminal as that of the wiring through which a voltage is supplied to a bias circuit and said electrostatic discharge protecting circuits for said amplifier (see pad 7 in fig. 4).

Referring to Claim 17, Tanaka also teaches said amplifier present on said edge portion of said semiconductor chip and arranged near the center of said edge portion (see fig. 5).

Referring to Claim 18, Tanaka also teaches said amplifier arranged at a corner part which is defined between said edge portion of said semiconductor chip and a crossing side which crosses said one edge portion (see pads 2', 6', and 7' in fig. 5).

Referring to Claim 19, Tanaka also teaches no wiring arranged between said electrode terminal and said edge portion of said semiconductor chip (see fig. 4).

Referring to Claim 20, Tanaka also teaches the wiring arranged from said electrode terminal linked with said control electrode of said transistor and one electrode of electrostatic discharge protecting which are provided for said transistor (see fig. 4 where it is known in the art that electrostatic discharge protecting are provided in most transistors today).

Referring to Claim 21, Tanaka also teaches the electrostatic discharge protecting circuit provided for said transistor connected to said first electrode and said second electrode of said transistor, respectively (see figs. 4 and 5).

Referring to Claim 23, Matsubara also teaches said semiconductor chip including electrostatic discharge protecting circuits connected through a first wiring to said plurality of electrode terminals connected with said transistor, and wherein none of said wirings, except for said first wiring, are arranged to traverse said wiring connected between said first electrode terminals and said first electrodes of said transistor, between said second electrode terminals and said second electrodes of said transistor, and between said third electrode terminals and said control electrodes of said transistor (see figs. 1, 5, and 6 where it is clear that none of said wirings traverse).

Referring to Claim 24, Matsubara also teaches one of said signal processing integrated circuits having no wiring, except for said first wiring, arranged to traverse said wirings connected between said first electrode terminals and said first electrodes of said transistor, between said second electrode terminals and said second electrodes of said transistor, and between said third electrode terminals and said control electrodes of said transistor (see figs. 1, 5, and 6 where it is clear that none of said wirings traverse).

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thompson, Tanaka, Matsubara, and Lysejko in view of Yamamoto et al. (US 6,308,047).

The combination of Thompson, Tanaka, Matsubara, and Lysejko does not teach the amplifier as a low-noise amplifier. Yamamoto teaches the amplifier as a low-noise amplifier (figs. 1 and 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teachings of Yamamoto to said system of Thompson in order to better reduce noise and interference.

Response to Arguments

5. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

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mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Yun whose telephone number is (571) 272-7860. The examiner can normally be reached on 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (571) 272-7848. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EY


Eugene Yun
Examiner
Art Unit 2682


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TECHNOLOGY CENTER 2600

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